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Design and Analysis of GDI Based Full Adder Circuit for Low Power Applications

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ABSTRACT:
Full adder circuit is an essential component for designing of various digital systems. It is used for different applications such as Digital signal processor, microcontroller, microprocessor and data processing units. Due to scaling trends and portability of electronic devices there is a high demand and need for low power and high speed digital circuits with small silicon area. So, design and analysis of low power and high performance adders are of great interest and any modification made to the full adder circuit would affect the performance of the entire system. This paper describes the design and analysis of GDI based 1-bit full adder circuit for low power applications. GDI technique is used to reduce power consumption, propagation delay while maintaining low complexity of logic design. Here we have introduced a 11-T GDI based full adder circuit which can be used for low power applications. The proposed circuit is better than the existing technique in terms of average power and speed with minimum area penalty. Simulations are based on BPTM model and have been carried out by Tanner EDA tool on 180nm, 90nm, 65nm and 45nm technology.
Keywords: Delay, Full adder, GDI (Gate Diffusion Input), Low Power.

I. INTRODUCTION

Binary addition is the basic operation found in most arithmetic components. Computation needs to be achieved by using area efficient circuits operating at high speed with low power consumption. Addition is the fundamental arithmetic operation and most fundamental arithmetic component of the processor is adder. Full Adder circuit plays an important role in low power applications. Hence the realization of full adders with low power and high performance is very essential. Obviously increasing the performance of 1-bit full adder circuit shows a great impact on increasing the performance of the entire system [1]-[2]. Designing low-power and high speed VLSI systems has emerged as highly in demand because of the fast growing technologies in communication and other battery power applications. Different design styles have been proposed to implement 1-bit adder cells [3]-[9].

One of the efficient low power technique known as Gate Diffusion Input (GDI) [10] is proposed by Morgenshtein. It is a genius and power efficient design with lesser number of transistor counts. In this paper we propose a new 11-T GDI based 1-bit full adder circuit for low power application by sacrificing the transistor count that reduces the average power consumption, considerably decreasing the delay compared to its base design i.e 10T full adder design. We have conducted simulations and results were analyzed on 180nm, 90nm, 65nm and 45nm BPTM using Tanner EDA tool.

The rest of paper is organized as follows. Section II describes the GDI based design. Proposed circuit is described in section III. Section IV shows the detail comparison and analysis of GDI based 1-bit full adder circuit on different technologies. Lastly conclusions and future scope are drawn in section V.

II. GDI BASED DESIGN

The basic GDI cell shown in Fig.1 was proposed by Morgenshtein [14]. It is a new technique for low power digital combinational circuit design. This technique reduces power consumption, propagation delay and area of digital circuits while maintaining low complexity of logic design.

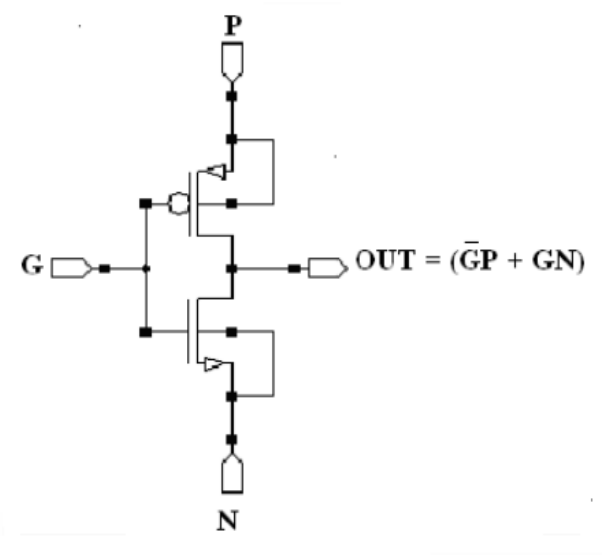

Figure.1 GDI Cell

The main difference between the CMOS and GDI based design is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. This feature gives the GDI cell two extra input pins for use which makes the GDI design more flexible than CMOS design.

GDI cell consists of three inputs - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both nMOS and PMOS are connected to N and P respectively. Table 1 shows different logic functions implemented by GDI logic [15] based on different input values. So by using GDI technique we can implement various logic functions with less power and high speed as compared to conventional CMOS design.

Table.1 Logic function of the basic GDI cell

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

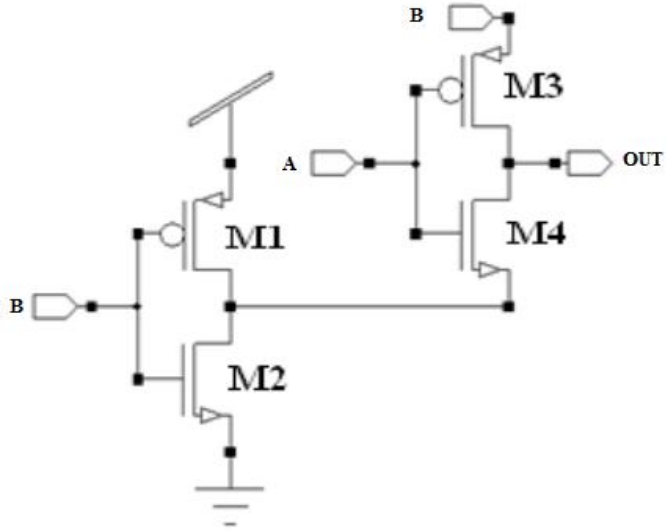

Figure. 2 GDI based XOR gate

Fig.2 shows the implementation of XOR gate using GDI technique [11]. It is the main building block of full adder circuit. So if we can optimize XOR gate then it can improve the overall performance of the 1 bit full adder circuit. It uses less number of transistors as compared to conventional design of XOR gate using CMOS logic. Fig.3 shows the detail circuit of GDI XOR based 10T Full Adder [11].

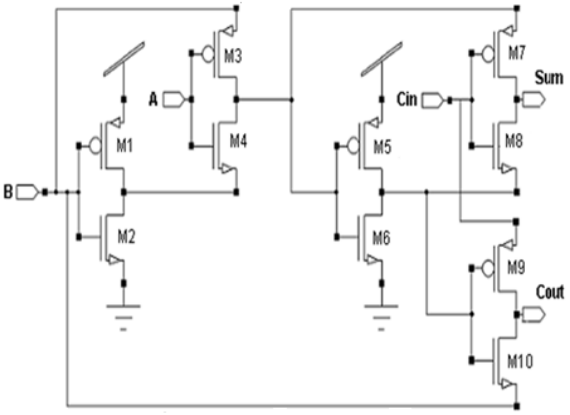

Figure. 3 GDI based 10T Full Adder

In fig 3 M1, M3, M5, M7, and M9 are the PMOS transistor whereas M2, M4, M6, M8, and M10 are the NMOS transistors. A, B and Cin are taken as input and output of the circuit is drawn from the Sum and Cout.

III. PROPOSED GDI BASED FULL ADDER

The proposed GDI 11-T Full Adder is shown in Fig. 4 M1, M3, M5, M7, and M9 are the PMOS transistor. M2, M4, M6, M8, and M10 are the NMOS transistors. A, B and Cin are taken as input and output of the circuit is drawn from the Sum and Cout. Here M11 is the sleep transistor which is responsible for reduction of average power consumption of the

entire circuit. When the circuit is in active mode sleep transistor is OFF and when the circuit is in standby mode then the sleep transistor is ON.

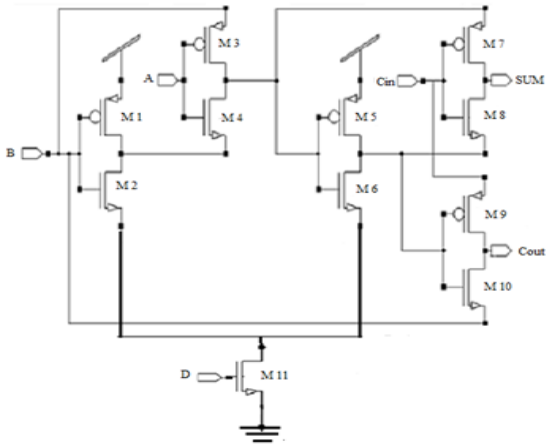

Figure. 4 Proposed GDI based 11T Full Adder.

By using modified GDI based 11-T full adder design, the power consumption is reduced to a greater extent and also the delay of the circuit compared to conventional GDI 10-T based full adder circuit [16].

IV. COMPARISION & ANALYSIS

Table.2 shows the variation of average power and delay of proposed GDI based 11-T full adder and existing GDI based 10-T full adder [16] with respect to different technologies at 27^0C. Comparison result shows that the average power of the proposed GDI technique is reduced by 48.74%, 36.89%, 5.52% and 2.65% at 180nm, 90nm, 65nm, and 45nm respectively. Fig. 5 clearly depicts that as technology decreases average power of the circuit also reduces up to certain extent. Fig. 6 shows that delay is reduced by 1.56%, 1.58%, 2.40% and 2.52% at 180nm, 90nm, 65nm, and 45nm respectively by comparing the proposed GDI technique with the existing GDI technique.

Table 2 Comparisons between the Proposed Technique and Existing Technique of GDI Based Full Adder

Technology	Average Power (μ w)			Delay (ns)		
	Existing Technique (10T)	Proposed Technique (11T)	Percentage Reduction (%)	Existing Technique (10T)	Proposed Technique (11T)	Percentage Reduction (%)
180nm	145.92	74.798	48.74	2.043	2.011	1.56
90nm	3.681	2.323	36.89	1.391	1.369	1.58
65nm	0.525	0.496	5.52	1.330	1.298	2.40
45nm	0.188	0.183	2.65	1.307	1.274	2.52

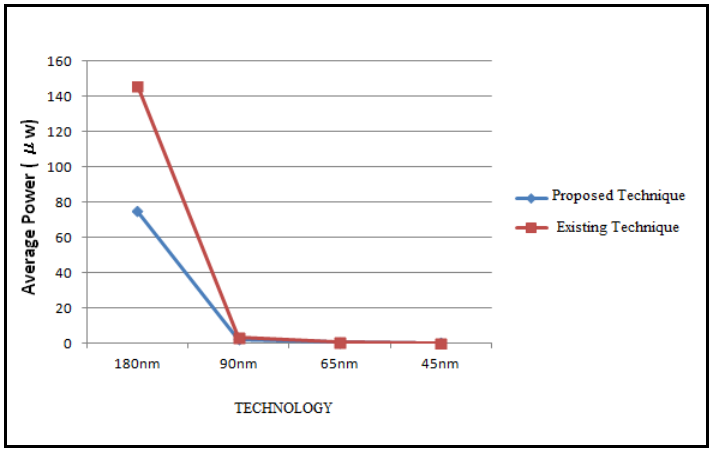

Figure. 5 Average power of Proposed and existing GDI based full adder in different technologies

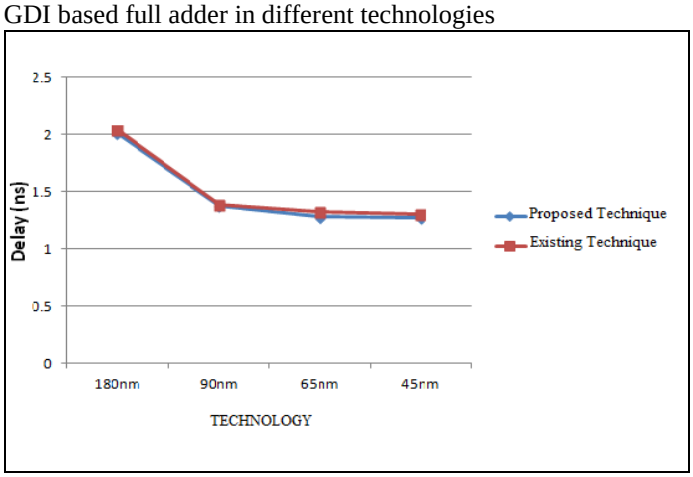

Figure.6 Delay of proposed and existing full adder in different technologies

V. CONCLUSION AND FUTURE SCOPE

Here a detail analysis of average power consumption and delay of proposed GDI based adder and the existing GDI based adder on different technologies is presented. Comparison of proposed GDI technique with the existing GDI technique shows that the average power is decreasing by 48.74%, 36.89%, 5.52% and 2.65% at 180nm, 90nm, 65nm, and 45nm respectively. In the same way delay is reduced by 1.56%, 1.58%, 2.40% and 2.52% at 180nm, 90nm, 65nm, and 45nm respectively. So by proper analysis of power and delay parameters we can easily use proposed GDI adder over existing adders for low power and high speed applications.

We hope that presented results will encourage the researchers for further research activities on GDI techniques. To reduce power of a GDI based adder cell some more circuit level power management techniques should be used so that it can be useful for low power applications. Implementation of different kinds of mixed and digital circuits have to be carried out in order to determine the fields of circuitry, where GDI is very much superior over other design styles.

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